REMARKS

At the time of the Office Action dated June 23, 2004, claims 1-20 were pending. Applicant acknowledges, with appreciation, the Examiner's indication that claims 5, 7, 12 and 14 would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. It is noted that claim 19 should have been indicated to be allowable in consideration of the recitations in claims 5 and 12. Applicant respectfully requests the Examiner to review claim 19.

Claims 1-4, 6, 8-11, 13 and 15-20 have been rejected under 35 U.S.C. §102(e) as being anticipated by Freerksen et al.

Following the January 14, 2004 Office Action, the Examiner maintained his position on the rejection of claims 1-4, 6, 8-11, 13 and 15-20, asserting that Freerksen et al. discloses a synchronous signal producing circuit, a processor system, and a method of producing a synchronous signal for synchronizing access by a processor and coprocessor to a shared memory, as claimed in the claims. Applicant respectfully traverses this rejection.

Applicant submits that Feerksen et al. does not disclose all the limitations recited in those claims. Specifically, the reference fails to show at least the limitation "a signal setting a processor to a wait state is issued based on a signal indicating that a coprocessor is executing a coprocessor instruction as well as a result of the comparison by said comparing circuit," as recited in independent claims 1, 8 and 15.

It is understood that Freerksen et al. discloses that a bus controller monitors a processor accessing particular data in a shared memory and broadcasts a retry transaction for that data (see column 8, lines 3-26). However, the reference is does not disclose, and the Examiner even did

not point out where Feerksen et al. discloses, that the bus controller uses a signal showing that a processor is executing instructions in order to broadcast the retry transaction. In contrast, the claimed "first logic circuit" is configured for "issuing a signal setting said processor to a wait state based on a signal indicating that the said coprocessor is executing a coprocessor instruction..." (emphasis added).

Therefore, Freerksen et al. does not disclose all the limitations recited in independent claims 1, 8 and 15 within the meaning of 35 U.S.C. §102. *See Helifix Ltd. v. Blok-Lok, Ltd.*, 208 F. 3d 1339, 54 USPQ2d 1299 (Fed. Cir. 2000); *Electro Medical Systems S.A. v. Cooper Life Sciences, Inc.*, 34 F.3d 1048, 32 USPQ2d 1017 (Fed. Cir. 1994).

It is noted that a dependent claim is not anticipated if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claim. Therefore, claims 2-4, 6, 9-11, 13 and 16-20 are patentable because they respectively include all the limitations of independent claims 1, 8 and 15. The Examiner's additional comments with respect to claims 2-4, 6, 9-11, 13 and 16-20 do not cure the argued fundamental deficiencies of Freerksen et al.

In more detail, Applicant stresses that Freerksen et al. does not disclose how to produce the signal setting the processor to the wait state. According to claims 2, 9 and 16, the signal is produced based on the signal indicating that the coprocessor is executing the coprocessor instruction, the result of the comparison and a signal indicating that locking of the shared memory is to be released. On the other hand, Freerksen et al. merely discloses, "To prevent processor 110 from retrieving the old version of data from main memory, bus controller 128, which snoops bus 150 (in particular, the command bus in system bus 150) and sees the read, broadcasts a retry transaction on the response bus" (column 8, lines 10-14). Freerksen et al. is

silent on the signals based on which the claimed invention produces the signal setting the processor to the wait state.

With respect to claims 3, 10 and 17, it is noted that Freerksen et al. does not disclose, among other things, that a bus error signal is issued based on the signal indicating that the coprocessor is executing the coprocessor instruction, the result of the comparison by the comparing circuit and a count value of the bus wait counter. The reference merely mentions, "Once this number [the number of retries allowed while a write is in a priory state] is reached (or exceeded), the bus controller will [shift] a write from a priority state to a normal state" (column 7, lines 10-17), and thus, does not disclose those signals used by the claimed invention for issuing the bus error signal.

For claims 4, 11 and 18, the Examiner asserted that Freerksen et al. in column 6, line 59 to column 7, line 16 discloses all the limitations recited in those claims. However, the cited portion merely discloses counting how many times each write has been rejected, determining if the write is in priority mode, and change from the priority write state to the normal write state based on how many times the write under the priority state is rejected. Therefore, it is apparent that Freerksen et al. does not disclose setting a wait number at the time when the signal setting the processor to the wait state sets the processor to the wait state, setting a wait number at the time of normal access by the processor, and selecting one of the wait numbers based on the signal indicating that the coprocessor is executing the coprocessor instruction as well as the result of the result of the comparison, as recited in claims 4, 11 and 18.

As to claims 6, 13 and 20, the Examiner pointed out that Freerksen et al. in column 8, lines 3-26 discloses the limitations recited in those claims. However, as discussed for claims 1, 8 and 15, the reference does not disclose using the signal indicating that the coprocessor is

executing the coprocessor instruction. Therefore, it is apparent that Freerksen et al. does not disclose holding information indicating that the coprocessor is executing the coprocessor instruction and producing the signal setting the processor to the wait state based on that information, as recited in claims 6, 13 and 20.

Applicant, therefore, respectfully solicits withdrawal of the rejection of claims 1-4, 6, 8-11, 13 and 15-20, and favorable consideration thereof.

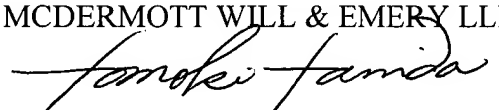
Conclusion.

Applicant submits that by the present Remarks, this application is placed in clear condition for immediate allowance. Accordingly, entry of the present Remarks, and favorable consideration, are respectfully solicited pursuant to the provisions of 37 C.F.R. §1.116. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, Examiner is requested to call Applicant's attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

MCDERMOTT WILL & EMERY LLP



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